

Attorney Docket No.: 00CON159P-C1

**REMARKS**

By the present amendment, claims 18 and 58 have been amended. Thus, after the present amendment, claims 18-33 and 58-66 remain in the present application.

Reconsideration and allowance of outstanding claims 18-33 and 58-66 in view of the above amendments and following remarks are requested.

**A. Rejection of Claims 18-20, 22-33, and 58-66 under 35 USC §102(b)**

The Examiner has rejected claims 18-20, 22-23, and 58-66 under 35 USC §102(b) as being anticipated by U.S. Patent Number 5,640,048 to Selna ("Selna"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 18 and 58, is patentably distinguishable over Selna.

The present invention, as defined by amended independent claim 18, discloses a structure including at least one signal via (second group of vias 250) providing an electrical connection between a device electrode of the chip and the PCB attached to a substrate. The structure further includes a plurality of separate thermally conductive vias (first group of vias 255) in the substrate that are coupled to a heat spreader. The heat spreader is directly attached to the bottom surface of the substrate.

The present invention, as defined by independent claim 58, discloses a structure including a heat spreader directly attached to a bottom surface of a substrate. The structure further includes a plurality of separate thermally conductive vias (first group of

Attorney Docket No.: 00CON159P-C1

vias 255) in the substrate providing a connection between the semiconductor chip and the heat spreader.

Referring to page 5 of the present application, due to the configuration of first group of vias 255, a good thermal and electrical connection from chip 100 to heat spreader 290 is provided. Moreover, referring to pages 6 and 7 of the present application, due to the configuration of second group of vias 250, no traces are necessary between the bond pads and the vias, so parasitic inductance is reduced. Due to this configuration, electrical inductance is reduced and space is saved since traces are not needed. The heat spreader attached to the PCB allows for a very low thermal resistance. Increased reliability is also achieved due to the claimed structure, because the mechanical stress or physical displacement on the plurality of lands 280, due to the heating and cooling of the structure, is decreased due to the heat spreader. Advantageously, as recited in the independent claims and disclosed in the present application, the heat spreader is directly attached to the bottom surface of the substrate.

Moreover, amended independent claims 18 and 58 recite language indicating that a die attach bond pad is attached to the top surface of the substrate and a downbond couples the chip to the die attach bond pad. As disclosed in the present application, page 8, electrical inductance is reduced by the presence of downbonds. In addition to electrical contact between semiconductor device chip 100 and die attach bond pad 240, additional connections can be made from preselected device electrodes 300 as needed, by down bonding from semiconductor device chip 100 to die attach bond pad 240. Downbonds

Attorney Docket No.: 00CON159P-C1

295 allow the preselected device electrodes of the semiconductor device chip to be electrically connected to die attach bond pad 240 and to heat spreader 290 by way of first group of vias 255. The utilization of downbonds 295 helps achieve minimal inductance because the length of the wire is minimal, and downbond 295 thus provides for a very good thermal and electrical path from semiconductor device chip 100 to the ground plane.

On the other hand, Selna simply teaches IC 12, printed circuit board material 52, 54, printed circuit board 18, and conductive and/or thermal vias 6A, 6B, and 6C. Selna teaches ground plane 20C connected to solder balls 14C. However, Selna does not disclose, teach, or even suggest the advantageous configuration defined by the independent claims, including the heat spreader directly attached to the substrate. Referring to column 1, lines 39 and 40, Selna teaches conductive trace 10C; however, according to Selna, conductive trace 10C is a trace and not a heat spreader. Furthermore, Selna does not even suggest that a die attach bond pad is attached to the top surface of the substrate and a downbond couples the chip the die attach bond pad.

For the foregoing reasons, Applicant respectfully submits that the present invention as defined by amended independent claims 18 and 58 is not taught, disclosed, or suggested by Selna. Thus, amended independent claims 18 and 58 are patentably distinguishable over Selna. As such, the claims depending from amended independent claims 18 and 58 are, *a fortiori*, also patentably distinguishable over Selna for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Attorney Docket No.: 00CON159P-C1

**B. Rejection of Claim 21 under 35 USC §103(a)**

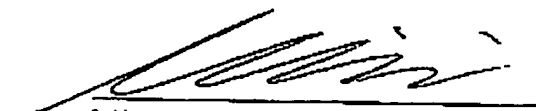
The Examiner has rejected claim 21 under 35 USC §103(a) as being obvious with respect to Selna. Applicant respectfully submits that claim 21 depends from amended independent claim 18 and thus, claim 21 should be allowed at least for the same reasons discussed above in conjunction with patentability of amended independent claim 18.

**C. Conclusion**

Based on the foregoing reasons, the present invention, as defined by amended independent claims 18 and 58, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 18-33 and 58-66 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 18-33 and 58-66 pending in the present application is respectfully requested.

Attorney Docket No.: 00CON159P-C1

Respectfully Submitted,  
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